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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/800,530	03/06/2001	Edward L. Schwartz	74451P127D10	4151

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EXAMINER	
SHERALI, ISHRAT I	

ART UNIT	PAPER NUMBER
2621	

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/800,530	EDWARD SCHWARTZ	
	Examiner	Art Unit	
	Sherali Ishrat	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *18 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/12/04 & 9/02/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment/Arguments

1. This action is in response to Applicant's amendment/arguments received on 10/18/2004.

Applicant's arguments are fully considered, however they are moot due to new grounds of rejection which was necessitated because of amendment to the claims. However for further discussion of Lynch et al. reference see the remarks section.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-24 are rejected under 35 USC § 112 as being indefinite.

Regarding independent claims 1, 9, 17 and 20, in lines 6-7, claims recite "wherein a value with all three bits having an identical logical value indicates that all bitplanes are to be truncated". Based on the specification and prior art of record, it is understood that with all three bits having logical one value indicates that all bitplanes are to be truncated when qanitizing bit-planes with a power of two step size $[2^N]$. However it is not clear and understood how with all three bits having logical zero value indicates that all bitplanes are to be truncated. Because based on the specification and prior art 2^{000} indicate no or zero bitplanes to be trancated. Therefore the amended limitation "wherein a value with all three bits having an identical logical [111/000] value indicates that all bitplanes are to be truncated" is vague and indefinite. Claims 1-8,

11-16, 18-19 and 21-24 are dependent on independent claims 1, 9, 17 and 20 therefore they are also rejected.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-24 are rejected under 35 USC § as being unpatentable over Lynch et al. (US 6,229,929) in view of Raghunath (US 5,946,349).

Regarding claims 1, 9, and 20 Lynch discloses receiving a sequence of image data to compress (See Lynch, Figure 4, col. 14, lines 24-25, Lynch shows receiving sequence of image data from storage [Figure 4, Block 110] to compress [Figure 4, Block 114];

specifying a scalar quantization with power of two step size (See Lynch, col. 14, lines 41-45, Lynch shows "performing quantization by a power of two" which is equivalent to quantization with power of two step size [2^N])

using three bit values to specify a number of bit planes to be truncate during the quantization (See Lynch, col. 14, lines 48-51, Lynch shows the number lower order bits are truncated/discarded using quantization by power of two [2^N] bit value to truncate will obviously depend on the value of "N" i.e N = 0, 1, 2.....n, the number of bit planes to be truncated/discarded and in col. 14, lines 5-6, Lynch shows 8-bits coefficients,

therefore the value of N can be [0, 1, 2, 3, 4, 5, 6 and 7) in which 'N' depends on the number of bits to be truncated and it is known that binary equivalent of [0, 1, 2, 3, 4, 5, 6, 7] is specified using three bit values of [000, 001, 010, 011, 100, 101, 110, 111] therefore based on 2^N quantization of 8-bit coefficients of truncating of bit plane values, Lynch shows three bit values specify a number of bit planes to be truncate during the quantization).

Lynch has not explicitly shown with all three bits having identical logical value indicates that all bit-plane are be truncated. In the system of Lynch when N = 7 OR 111 all bits would be truncated because Lynch is using 8-bit data values.

However in the same field of endeavor Raghunath shows quantization of coefficients using 2^N (Raghunath, col. 3, lines 65-67 thru col. 4, lines 1-2, "coefficient values are represented by positional bits corresponding to increasing or decreasing powers of two which is equivalent 2^N") and shows with all bits having identical logical value indicates that all bit-plane are be truncated (Raghunath, Figure 3, col 5, lines 33-40, "Figure 3 shows coefficient is operated by bit truncation function which causes least significant bits to be dropped. That truncated coefficients is sent to a decision function which looks to see if the bit representation of the truncated coefficients [N] is all "1"s and if so operates to reset the value of coefficients to zero" which is equivalent to all bits having identical logical value indicates that all bit-plane are be truncated).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the teaching of Raghunath of truncating all bits of coefficients in the system of Lynch when all bits of 8-bit coefficients [111]] having

identical logical value because such a system provide discarding or resetting small positive coefficient thereby reducing storage needed in an image processing circuit.

Regarding claims 2, 10 and 19, Lynch disclose coding bitplanes specified for the scalar quantization (See Lynch, col. 14, lines 48-51, Lynch shows the number lower order bits are truncated/discarded using quantization by power of two [2^N] " transform coefficients in the system of Lynch are coded by discarding lower order bits which is equivalent of coding bitplanes specified for the scalar quantization).

Regarding claims 3, and 11 Lynch disclose non-specified bit planes are not coded (See Lynch, col. 14, lines 48-51, Lynch shows the number lower order bits are truncated/resetted using quantization by power of two [2^N] " transform coefficients in the system of Lynch are coded by truncating lower order bits and thereby higher order bits are not discarded and therefore not coded).

Regarding claims 4,12 and 21-24, Lynch discloses all bit planes are truncated when each of three bits representing the three bit value has a logical value one (See Lynch, col. 14, lines 48-51, Lynch shows the number bits are truncated/discarded using quantization by power of two [2^N], in the system of Lynch if N =7 and binary equivalent of 7 is 111 thereby all bits will be discarded if transform coefficient is 8-bit level and Raghunath, Figure 3, col 5, lines 33-40, states "Figure 3 shows coefficient is operated by bit truncation function which causes least significant bits to be dropped. That truncated coefficients is sent to a decision function which looks to see if the bit representation of the truncated coefficients [N] is all "1"s and if so operates to reset the

value of coefficients to zero" which is equivalent to all bits having identical logical value indicates that all bit-plane are be truncated).).

Regarding claims 5 and 13, Lynch discloses the three bit value specify 0, 1, 2, 3, 4, 5, 6 or all bit planes are discarded (See Lynch, col. 14, lines 48-51, Lynch shows the number bits are truncated/discarded using quantization by power of two [2^N], depending on the value of N (0, 1...6, 7) and using three bit binary value to represent 0, 1, ...6, 7 it will discard 0, 1, 2, 3, 4, 5, 6 or all bit planes depending on the value of N it is known that binary equivalent of [0, 1, 2, 3, 4, 5, 6, 7] is specified using three bit values of [000, 001, 010, 011, 100, 101, 110, 111]).

Regarding claims 6 and 14, Lynch discloses specifying scalar quantization comprise specifying quantization for motion video sequence (See Lynch, col. 14, lines 48-51, Lynch shows the numer bits are truncated/discarded using quantization by power of two [2^N], and figure 4, Lynch shows transform coding of motion video).

Regarding claims 7 ,15, and 18 Lynch has shown video sequence as discussed above. Lynch however has not explicitly disclosed video sequence comprise JPEG 2000 standard video sequence. However Lynch shows transform coding of video sequence as show in figure 4 and shows variable length coding on col. 14 , lines 54-56 which are also used in the JPEG 2000 standard video sequence therefore it would be obvious in the system of Lynch that video sequence comprise JPEG 2000 standard.

Regarding claims 8 and 16, Lynch disclose writing the three bit values to a controller to cause to controller to control compression hardware (See Lynch, col. 14, lines 48-51, Lynch shows the number bits are truncated/discarded using quantization by

power of two [2^N], depending on the value of N (0, 1...6, 7) and using three bit binary value to represent 0, 1, ...6, 7 it will discard 0, 1, 2, 3, 4, 5, 6 or all bit planes depending on the value of N and col. 14, lines 52-55, Lynch shows after quantization [discarding/truncating of bits using 2^N quantization] of transform coefficients are entropy encoded. It is obvious that those bits of the block are coded which are not discarded therefore in the system of Lynch controller of compression has knowledge of N [three bit values] to the quantize the coefficients and compressed the quantized coefficients).

Regarding claim 17, Lynch discloses the difference between claim 1 and 17, which is the following:

a compressor coupled to the controller to compress the sequence image data to create compressed data (See Lynch, col. 14, lines 25-30, blocks [sequence of image] are compressed using linear/non-linear transform coding by performing sequences of passes. Lynch shows blocks are compressed by performing sequences of passes therefore Lynch compressor is coupled to controller so the sequences of passes can be controlled),

the compressor comprising quantizer (See Lynch, col. 14, lines 36-38, compressed block are quantized. Lynch compressor comprises quantizer because in the system of Lynch compressed blocks are quantized).

Remarks

6. In the amendment filed on 10/18/2004. Applicant argued the following:

Lynch fail to disclose number of bits in power of two step using three bits and value having all bits as the same logical value indicate that all bit-planes are to be truncated.

a. Examiner disagree with applicant's interpretation of Lynch reference. Lynch in col. 14, lines 48-51, shows the number lower order bits are truncated/discarded using quantization by power of two [2^N] bit value to truncate will obviously depend on the value of "N" i.e N = 0, 1, 2.....n, the number of bit planes to be truncated/discarded and in col. 14, lines 5-6, Lynch shows 8-bits coefficients, therefore the value of N can be [0, 1, 2, 3, 4, 5, 6 and 7) in which 'N' depends on the number of bits to be truncated and it is known that binary equivalent of [0, 1, 2, 3, 4, 5, 6, 7] is specified using three bit values of [000, 001, 010, 011, 100, 101, 110, 111] therefore based on 2^N quantization of 8-bit coefficients of truncating of bit plane values, Lynch shows three bit values specify a number of bit planes to be truncate during the quantization). Lynch has not explicitly shown with all three bits having identical logical value indicates that all bit-plane are be truncated. In the system of Lynch when N = 7 OR 111 all bits would be truncated because Lynch is using 8-bit data values. Furthermore with regard to the amended limitation with all three bits having identical logical value indicates that all bit-plane are be truncated, Raghunath, col. 5, lines 33-40, states "Figure 3 shows coefficient is operated by bit truncation function which causes least significant bits to be dropped. That truncated coefficients is sent to a decision function which looks to see if the bit representation of the truncated coefficients [N] is all "1"s and if so operates to reset the value of coefficients to zero"

which is equivalent to all bits having identical logical value indicates that all bit-plane are be truncated.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sherali Ishrat whose telephone number is 703-308-9589. The examiner can normally be reached on 8:00 AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Boudreau can be reached on 703-305-4706. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ishrat Sherali

Patent Examiner

Art Unit 2621

January 26, 2004

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